

WHAT IS CLAIMED IS:

1 1. An EEPROM integrated circuit structure, the structure comprising:
2 a substrate including a surface region, the surface region being provided within a first cell
3 region; a gate dielectric layer of first thickness overlying the surface of the substrate
4 region; a select gate overlying a first portion of the gate dielectric layer; a floating gate
5 floating gate overlying a second portion of the gate dielectric layer and coupled to the
6 select gate;
7 an insulating layer overlying the floating gate; a control gate
8 overlying the floating gate overlying the insulating layer and coupled to the floating gate;
9 a tunnel window provided in a stripe configuration within a portion of the gate dielectric
10 layer, the portion of the gate dielectric layer being of a second thickness, the second
11 thickness being less than the first thickness.

1 2. The structure of claim 1 wherein the gate dielectric layer comprises
2 a silicon dioxide.

1 3. The structure of claim 1 wherein the tunnel window is characterized
2 by a width of less than 0.25 microns.

1 4. The structure of claim 1 wherein the insulating layer is an ONO
2 layer coupled between the floating gate and the control gate.

1 5. The structure of claim 1 wherein the floating gate has a design
2 width of 1.5 microns.

1 6. The structure of claim 1 wherein the tunnel window is provided
2 using a phase shift mask.

1 7. The structure of claim 1 wherein the stripe configuration extends
2 through a plurality of cells, each of the cells being separated by a field oxide region.

1 8. The structure of claim 1 wherein the substrate is a semiconductor
2 wafer.

1 9. The structure of claim 1 wherein the select gate, floating gate, and
2 control gate are provided within a cell region, the cell region being provided within an
3 isolation region.

1 10. The structure of claim 1 wherein the stripe configuration runs
2 through the first cell region to other cell regions numbered from 2 through N, where N is
3 an integer greater than 2.

1 11. An EEPROM integrated circuit structure, the structure comprising:
2 providing a substrate including a surface region, the surface region being provided within
3 a first cell region; forming a gate dielectric layer of first thickness overlying the surface of
4 the substrate region; patterning the gate dielectric layer to form a plurality of stripes, each
5 of the stripes being characterized by a second thickness, the second thickness being less
6 than the first thickness, each of the stripes having a predetermined width and a
7 predetermined length, at least one of the stripes including a stripe portion traversing
8 through a portion of the first cell region and other cell regions;
9 forming a floating gate overlying a portion of the gate dielectric
10 layer, the portion of the gate dielectric layer including the stripe portion traversing through
11 the portion of the gate dielectric layer;
12 forming an insulating layer overlying the floating gate; forming a
13 control gate overlying the floating gate overlying the insulating layer and coupled to the
14 floating gate; and
15 wherein the stripe portion traverses through the portion of the first
16 cell region includes a tunnel window for a memory device.

1 12. The method of claim 11 wherein the gate dielectric layer comprises
2 a silicon dioxide.

1 13. The method of claim 11 wherein the tunnel window is characterized
2 by a width of less than 0.25 microns.

1 14. The method of claim 11 wherein the insulating layer is an ONO
2 layer coupled between the floating gate and the control gate.

1 15. The method of claim 11 wherein the floating gate has a design
2 width of 1.5 microns.

1 16. The method of claim 11 wherein the tunnel window is provided
2 using a phase shift mask.

1 17. The method of claim 11 wherein the stripe configuration extends
2 through a plurality of cells, each of the cells being separated by a field oxide region.

1 18. The method of claim 11 wherein the substrate is a semiconductor
2 wafer.

1 19. The method of claim 11 wherein the floating gate and the control
2 gate are provided within a cell region, the cell region being provided within an isolation
3 region.

1 20. The method of claim 11 wherein the stripe configuration runs
2 through the first cell region to the other cell regions, the other cell regions being numbered
3 from 2 through N, where N is an integer greater than 2.